

Second, set the lpGBT mode on TRX, enable the uplink and downlink EC channel, click on Quick configuration and send again the configuration to the lpGBT:

Chip Mode

LpGBT Mode: OFF, TX, RX, **TRX**

Transmitter mode

Tx Data Rate: 5Gbps, **10Gbps**

Tx Encoding: **FEC5**, FEC12

Uplink EPRX

Data rate: OFF, 320, 640, 1280

option: TERM, AC Bias

Uplink EC

Eport state: Disable, **Enable**

Track mode: Static, Auto Startup, Continuous, Continuous Init Phase

Channel option: TERM, AC Bias, INV

Phase: [Slider]

Downlink EPTX

Data rate: OFF, 80, 160, 320

Drive strength: 0 mA

Pre-emp mode: Disabled

Pre-emp strength: 0 mA

Pre-emp width: 120 ps

Downlink EC

Eport state: Disable, **Enable**

Drive strength: 0 mA

High speed links polarity

Invert high speed data output: Disable, **Enable**

Invert high speed data input: **Disable**, Enable

Line Driver

Modulation Current: [Slider] 8.77 mA

Pre-emphasis: Disable, Enable

Pre-emphasis Current: [Slider] 4.38 mA

Equalizer

	0	-3.6	-3.6	-9.5	dB
Attenuation	0	-3.6	-3.6	-9.5	dB
Capacitance	0	70	70	140	fF
Resistance 0	0	3	4.7	7.1	k
Resistance 1	0	3	4.7	7.1	k
Resistance 2	0	3	4.7	7.1	k
Resistance 3	0	3	4.7	7.1	k

Eye Opening Monitor

Measure

Invert the high-speed link polarity for the output (in the High Speed settings)

AND: in the Registers settings, load the config file, even if there's no AMAC chip on module, to set the clock.

First, select the components of the setup:

Select Platform

PiGBT mode: Dummy LpGBT, **Real LpGBT**

Hardware: **VLDB + board**, Other support

I2C address: 115

Ok

The only address available to select

lpGBT status

lpGBT version: 0

I2C address: 115

Chip ID: F94BF306

Mode: MODE 10G FEC5 TRX

Lock Mode: RECOVERED REF CLK

State: **READY**

Watchdog and Timeout

Watchdog PLL: disabled, **enabled**

Timeout PLL: 1000 ms

Process monitors

Channel	Value
Channel 1	2589902
Channel 2	2611775
Channel 3	2586644
Channel 4	2594802