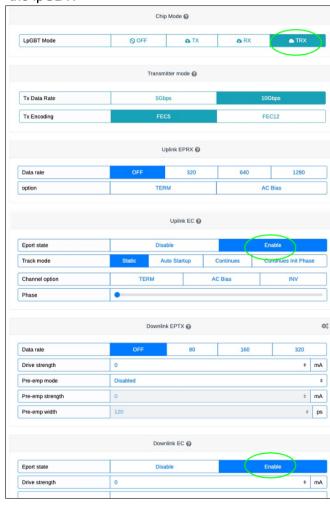
Second, set the IpGBT mode on TRX, enable the uplink and downlink EC channel, click on Quick configuration and send again the configuration to the IpGBT:



High speed links polarity @ Invert high speed data output Invert high speed data input Disable Line Driver @ Modulation Current 8.77 mA Pre-emphasis 4.38 mA Pre-emphasis Current Equalizer @ Attenuation -3.6 -3.6 140 fF Capacitance 70 70 Resistance 0 3 4.7 7.1 4.7 Resistance 1 3 7.1 4.7 7.1 Resistance 2 3 3 4.7 7.1 Resistance 3 Eye Opening Monitor @

Invert the high-speed link polarity for the output (in the High Speed settings)

AND:
in the
Registers
settings, load
the config
file, even if
there's no
AMAC chip
on module,
to set the
clock.

	IpGBT status	
lpGBT version	0	
I2C address	115	
Chip ID	F94BF306	
Mode	MODE 10G FECS TRX	
Lock Mode	RECOVERED REF CLK	
State	READY	
Watehdae Di I	Watchdog and Timeout ⊘	C nobled
Watchdog PLL	Watchdog and Timeout ⊚ □ disabled	© enabled
Watchdog PLL Timeout PLL		○ enabled
	Φ disabled	
Timeout PLL	© disabled 1000 Process monitors	
Timeout PLL	© disabled 1000 Process monitors 2589902	

First, select the components of the setup:

PiGBT mode	Dummy LpGBT	Real LpGBT
Hardware	VLDB + board	Other support
I2C address	115	

The only address available to select